UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/938,496	08/27/2001	Hideo Miyake	1614.1181	2883

21171   7590   02/08/2006

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EXAMINER
MARTIN, CIARA A

ART UNIT	PAPER NUMBER
2157	

DATE MAILED: 02/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	09/938,496	MIYAKE ET AL.
	Examiner	Art Unit	
	Ciara Martin	2157	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
   Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 November 2005*.

2a)☐ This action is **FINAL.**   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-13 and 15-19* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5, 7-13, 15-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☒ All   b)☐ Some * c)☐ None of:

      1.☒ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/19/05*.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1.   A request for continued examination under 37 CFR 1.114, including the fee set

forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this

application is eligible for continued examination under 37 CFR 1.114, and the fee set

forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action

has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on

November 23, 2005 has been entered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2.   Claims 1-5, 7-13, 15-19 are rejected under 35 U.S.C. 102(e) as being anticipated

by Lai at al. US 6,216,193.

As per claim 1, Lai teaches a computer which processes an interrupt when an

instruction in a program is executed, said computer comprising:

a data holding part which holds data at a time when said interrupt starts to occur,

said data holding part holding data for continuing an instruction that is not a cause of

said interrupt and that is interrupted due to occurrence of said interrupt (6:60-67; 7:12-

32; 12:16-22; abstract; Lai discloses re-supplying data lost during an interruption by a target initiated termination request. The target that initiated the interrupt is not necessarily the target that receives the lost data).

As per claim 2, Lai teaches the computer as claimed in claim 1, wherein said data holding part includes a plurality of registers (Fig. 3, element 78; array holding registers).

As per claim 3, Lai teaches the computer as claimed in claim 2, said computer further comprising flags each of said flags indicating whether said data is held in said register (13:39-48).

As per claim 4, Lai teaches the computer as claimed in claim 1, said computer further comprising a data storing part, wherein said data holding part holds said data to be stored in said data storing part at a time when said interrupt occurs while a store instruction is executed, said store instruction requesting that said data is stored in said data storing part (7:13-32).

As per claim 5, Lai teaches the computer as claimed in claim 1, wherein said data holding part holds an instruction address of an instruction which causes said interrupt (3:1-22).

As per claim 7, Lai teaches the computer as claimed in claim 1, wherein said data holding part holds an effective address of a load instruction or a store instruction when said interrupt occurs while said load instruction or said store instruction is executed (7:13-32).

As per claim 8, Lai teaches the computer as claimed in claim 1, wherein said data is used for recovery from said interrupt (7:13-32).

As per claim 9, Lai teaches a control method of a computer which processes an interrupt when an instruction in a program is executed, said method comprising the step of:

holding data at a time when said interrupt starts to occur, said data holding part holding data for continuing an instruction that is not a cause of said interrupt and that is interrupted due to occurrence of said interrupt (6:60-67; 7:12-32; 12:16-22; abstract; Lai discloses re-supplying data lost during an interruption by a target initiated termination request. The target that initiated the interrupt is not necessarily the target that receives the lost data)..

As per claim 10, Lai teaches the control method as claimed in claim 9, wherein said data is held in a plurality of registers and said data is used for recovery from a plurality of interrupts (Fig. 3, element 78; array holding registers).

As per claim 11, Lai teaches the control method as claimed in claim 10, wherein flags are used in which each of which flags indicates whether said data is held in said register (13:39-48).

As per claim 12, Lai teaches the control method as claimed in claim 9, said control method comprising the step of: holding said data to be stored in a data storing part in said computer at a time when said interrupt occurs while a store instruction is executed, said store instruction requesting that said data is stored in said data storing part (7:13-32).

As per claim 13, Lai teaches the control method as claimed in claim 9, said
control method comprising the step of: holding an instruction address of an instruction
which causes said interrupt (3:1-22).

As per claim 14, Lai teaches the control method as claimed in claim 9, said
control method comprising the step of: holding data which indicates a factor of said
interrupt.

As per claim 15, Lai teaches the control method as claimed in claim 9, said
control method comprising the step of: holding an effective address of a load instruction
or a store instruction when said interrupt occurs while said load instruction or said store
instruction is executed (7:13-32).

As per claim 16, Lai teaches the control method as claimed in claim 9, wherein
said data is used for recovery from said interrupt (7:13-32).

As per claim 17, Lai teaches 17 a computer processing method comprising:

holding in a memory at least an address of an instruction in an operation when
interrupt processing that is not caused by the instruction causes the operation to halt
(6:60-67; 7:12-32; 12:16-22; abstract; Lai discloses re-supplying lost data and address
from a holding register during an interruption by a target initiated termination request.
The target that initiated the interrupt is not necessarily the target that receives the lost
data).

As per claim 18, Lai teaches the computer processing method according to claim
17, further comprising continuing the operation by executing the instruction held in the
memory after the interrupt processing is discontinued (7:12-32; 12:16-22, abstract).

As per claim 19, Lai teaches the computer processing method according to claim 17, wherein the address of the instruction is held in the memory when the interrupt processing starts to occur (7:12-32; 12:16-22, abstract).

Response to Arguments

Applicant's arguments filed on November 23, 2005 have been fully considered but they are not persuasive.

Applicant argues in substance that A) Lai does not suggest holding data for continuing an instruction that is not a cause of the interrupt and that is interrupted due to the occurrence of the interrupt.

In response to A): Lai discloses re-supplying lost data and address from a holding register during an interruption by a target initiated termination request. The target that initiated the interrupt is not necessarily the target that receives the lost data (6:60-67; 7:12-32; 12:16-22; abstract).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ciara Martin whose telephone number is 571-272-7507. The examiner can normally be reached on M-F 6:30- 4:00 with second Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ario Etienne can be reached on 571-272-4001. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

CM
1/24/06

ARIO ETIENNE
PRIMARY EXAMINER